

PFC Voltage Loop Compensation

We assume a multiplier input voltage, V_{mult} . I_{mout} is given by

$$I_{mout} = (V_{mult} - 1)I_{ac}/K.V_{ff}^2$$

Where K is 1 such that

$$I_{mout} = (V_{mult} - 1)I_{ac}/V_{ff}^2$$

Differentiating with respect to V_{mult} gives the response as

$$dI_{mout}/dV_{mult} = I_{ac}/V_{ff}^2$$

We already have,

$$I_{AC} = V_{IN}/R_{iac}$$

$$\begin{aligned} V_{FF} &= I_{AC}.R_{ff}/2 \\ &= V_{IN}.R_{ff}/2R_{iac} \end{aligned}$$

Substituting

$$dI_{mout}/dV_{mult} = 4R_{iac}/V_{IN}.R_{ff}^2$$

The input current response is

$$\begin{aligned} dI_{IN}/dV_{mult} &= dI_{mout}.R_{mult}/R_{sns} \\ &= 4R_{iac}.R_{mult}/V_{IN}.R_{ff}^2.R_{sns} \end{aligned}$$

With the output current response being

$$dI_{OUT}/dV_{mult} = dI_{IN}(1 - D)$$

Since

$$D = (V_{OUT} - V_{IN})/V_{OUT}$$

$$\begin{aligned} (1 - D) &= 1 - (V_{OUT} - V_{IN})/V_{OUT} \\ &= V_{IN}/V_{OUT} \end{aligned}$$

Giving

$$\begin{aligned} dI_{OUT}/dV_{mult} &= dI_{IN}.V_{IN}/V_{OUT} \\ &= 4R_{iac}.R_{mult}/V_{OUT}.R_{ff}^2.R_{sns} \end{aligned}$$

Converted to a voltage across the output capacitor

$$\begin{aligned} dV_{OUT}/dV_{mult} &= -j.dI_{OUT}/2\pi.f.C_{OUT} \\ &= -j.4R_{iac}.R_{mult}/2\pi.f.C_{OUT}.V_{OUT}.R_{ff}^2.R_{sns} \end{aligned}$$

Sampled by the voltage feedback divider

Approximating $V_{REF}/(V_{OUT}+V_{REF})$ as V_{REF}/V_{OUT}

$$\begin{aligned}dV_{fb}/dV_{mult} &= -j.4R_{iac}.R_{mult}.V_{REF}/2\pi.f.CO_{UT}.V_{OUT}^2.R_{ff}^2.R_{sns} \\ &= -j.2R_{iac}.R_{mult}.V_{REF}/\pi.f.R_{sns.CO_{UT}}(V_{OUT}.R_{ff})^2\end{aligned}$$

Call this the control to output response, G_{co}

The voltage error amplifier is loaded by the ground pole capacitor, C_P . With a forward transconductance of g_{fs} A/V its gain is

$$G_{vea} = -j.g_{fs}/2\pi.f.C_P.$$

The loop gain is

$$\begin{aligned}GL &= G_{vea}.G_{co} \\ &= (-j.g_{fs}/2\pi.f.C_P)(-j.2R_{iac}.R_{mult}.V_{REF}/\pi.f.R_{sns.CO_{UT}}(V_{OUT}.R_{ff})^2)\end{aligned}$$

Assuming a line frequency of 50Hz the equivalent rectified frequency is 100Hz. Targeting a crossover frequency, f_{co} , of 20Hz and setting GL to unity at this frequency allows C_{gnd} to be calculated as.

$$C_P = (g_{fs}/2\pi.f_{co})(2R_{iac}.R_{mult}.V_{REF}/\pi.f_{co}.R_{sns.CO_{UT}}(V_{OUT}.R_{ff})^2)$$

In the circuit under consideration

$$\begin{aligned}g_{fs} &= 100\mu \\ f_{co} &= 20\text{Hz} \\ R_{iac} &= 720\text{K} \\ R_{mult} &= 470\text{R} \\ V_{REF} &= 7\text{V5} \\ R_{sns} &= 0\text{R}025 \\ CO_{UT} &= 470\mu\text{F} \\ V_{OUT} &= 400\text{V} \\ R_{ff} &= 24\text{K}\end{aligned}$$

Giving

$$\begin{aligned}C_P &= 59.37\text{nF} \\ &= 47\text{nF}\end{aligned}$$

R_p is used to force this DC pole out to half the crossover frequency or 10Hz.

$$\begin{aligned}R_p &= 1/2\pi.f_p.C_P \\ &= 338\text{K} \\ &= 330\text{K}\end{aligned}$$

C_Z breaks the DC path at 2Hz making C_Z 10 times C_P or 470n

Job Done..... and a damn site better than.....

PFC voltage loop

The voltage loop must crossover at a lower frequency than twice the ac line frequency so that voltage corrections will not interfere with power factor correction. Second harmonic ripple from the sensed VC1 voltage directly results in third harmonic distortion on the ac line, similar to ripple on the VFF voltage.